

REMARKS/ARGUMENTS

Claims 1-24 are pending in the present application. Claims 1-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Morrison et al. (Pub. No.: US 2002/0038398) in view of Sarangdhar (US Patent RE 38,388).

Applicant's respectfully submit that the cited references do not teach, suggest or disclose “[a] method for executing a locked bus transaction in a multi-node system, comprising: initiating a locked-bus transaction at a bus agent; transmitting a locked-bus request to a first node controller; and deferring the locked-bus transaction at the bus agent by said first node controller” (e.g. as recited in claim 1).

The Office Action asserts:

Morrison disclose all the limitations as above except deferring the locked-bus transaction at the bus agent by said first node controller. However, Sarangdhar discloses a memory agent or I/O agent in the computer system may defer a response on any request other than a bus locked request, another deferred reply transaction, or a cache line write designated for explicit writeback. (col. 11, lines 52-55) Furthermore, Sarangdhar discloses at col. 10, lines 26-38) a transaction can be retried when the DEFER# signal asserted. A bus agent incapable of supporting a deferred response will provide a retry response if unable to provide the required response at the time of the response phase.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Sarangdhar's teaching into Morrison's system so as to minimize cost for bus agents unable to accommodate split transactions. (col. 2, lines 40-50)

Column 11 lines 52-55 state –

In one embodiment, a memory agent or I/O agent in the computer system may defer a response on any request other than a bus locked request, another deferred reply transaction, or a cache line write designated for explicit writeback.

Column 13 lines 1-7 state:

A transaction can be retried when the DEFER# signal is asserted and the HITM# signal is non-asserted during the Snoop Phase followed by a retry response during the Response Phase. That is, a bus agent incapable of supporting a deferred response will provide a retry response if unable to provide the required response at the time of the Response Phase.

When Defer Enable (DEN#) is asserted, the transaction can be completed in-order, can be retried, or deferred. When a transaction is to receive a deferred reply, the DEFER# signal

Application No.: 09/751,623
Amendment Date: February 22, 2005
Reply to Office Action dated: November 19, 2004

is asserted (while the HITM# signal is deasserted) during the Snoop Phase followed by a deferral response in the Response Phase.

Column 2 lines 40-50 state:

One problem with such a scheme is that the unnecessary polling increases bus traffic. It is desirable to reduce bus traffic when providing a retry response. Note that it is also desirable to minimize cost for bus agents unable to accommodate split transactions.

The present invention provides a method and apparatus for implementing such a bus protocol. The protocol of the present invention provides a method and apparatus for accommodating split transactions without the use of separate token buses and without the increased number of pins associated with them.

Applicants respectfully submit that the cited references do not teach suggest or disclose “[a] method for executing a locked bus transaction in a multi-node system, comprising ... *deferring* the locked-bus transaction at the bus agent by said first node controller” (emphasis added). Applicant agrees with the Office Action assertion that Morrison does not disclose deferring of the locked bus transaction (deferring meaning delaying *and* retrying until the locked bus transaction is accepted). Further support of the operation of deferring can be found at page 7 line 16 which states: “In block 203, the node controller 115 does not accept this locked-bus transaction (*e.g., by asserting an appropriate signal, DEFER# in this embodiment, and by giving a retry response*), causing the processor to retry the locked-bus transaction until it is accepted” (emphasis added).

The Office Action asserts Sarangdhar discloses a memory agent or I/O agent in the computer system may defer a response on any request other than a bus locked request, another deferred reply transaction, or cache line write designated for explicit writeback. Furthermore, the office action states Sarangdhar discloses a transaction can be retried when the DEFER# signal is asserted. Applicants respectfully disagree. The cited sections of Sarangdhar merely disclose a) a computer system that may defer *a response*

when *there is no bus locked request, a second deferred reply transaction or a cache line write designated for explicit writeback* and b) a generic DEFER capability upon which a transaction is retried. However, it is clear that the cited section of Sarangdhar that Sarangdhar fails to disclose at least two recited elements of independent claim 1: a) a multi-node system *deferring a locked bus transaction at the bus agent* and b) the deferral being performed *by the said first node controller*. There is no disclosure of at least either of these two elements in the Sarangdhar reference.

Moreover, despite the fact that Morrison and Sarangdhar fail to disclose multiple elements of independent claim 1, it is also noted that there is no teaching, suggestion or disclosed motivation to combine the teachings of Sarangdhar and Morrison. A critical step in analyzing the patentability of claims pursuant to section 103(a) is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. *See In re Kotzab*, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (*citing In re Dembicza*k, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one “to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher.” *Kotzab*, 55 USPQ2d at 1316 (*quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)). It is clear that there is no actual teaching or suggestion to combine these two references except beyond impermissible hindsight. Accordingly, reconsideration and withdrawal of the rejection of claims 1-9 and 11-27 under 35 U.S.C. § 103(a) is respectfully requested.

Application No.: 09/751,623
Amendment Date: February 22, 2005
Reply to Office Action dated: November 19, 2004

Since each and every limitation of the embodiment of claim 1 is not disclosed in, nor taught by cited references, reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 103(a) is respectfully requested. Independent claims 10, 19, and 21 contain similar allowable limitations and therefore the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn as well. Dependent claims 2-9, 11-18, 20 and 22-24 depend from allowable independent claims, and therefore are in condition for allowance.

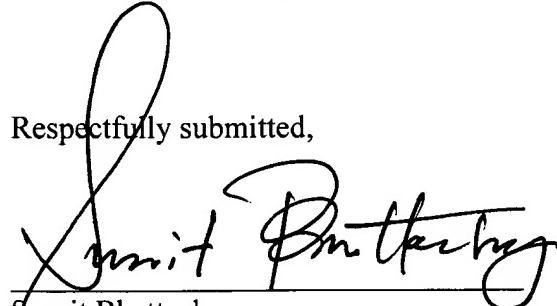
For at least the above reasons, Applicants respectfully submit that the present case is in condition for allowance and respectfully requests that the Examiner issue a notice of allowance.

The Office is hereby authorized to charge any fees determined to be necessary under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Kenyon & Kenyon

Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,


Sumit Bhattacharya
(Reg. No. 51,469)

Attorneys for Intel Corporation

Dated: February 22, 2005

KENYON & KENYON
333 W. San Carlos Street
Suite 600
San Jose, CA 95110
Tel: (408) 975-7500
Fax: (408) 975-7501